

REMARKS

Claims 5-13 and 26-28 are pending in this application.

The Examiner has objected to the Abstract because the Abstract contains the undefined acronym "MAC". Applicants have herewith amended the Abstract to define the acronym "MAC" as "multiply-accumulate block" and to correct a minor typographical error. The amendments are fully supported and justified by the originally filed specification. In view of these amendments, applicants respectfully request that the objection to the Abstract be withdrawn.

Claims 5-13 and 26-28 have been rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. This rejection is respectfully traversed.

Applicants respectfully submit that this rejection is misplaced. The Examiner bases the rejection on an alleged lack of a "concrete, useful, and tangible result" because the claims "merely disclose elements for performing mathematical function [sic] without disclosing a practical application . . . ." However, according to MPEP § 2106, which subsumes the November 2005 interim guidelines cited by the Examiner, an inquiry regarding a "useful, concrete and tangible result" is made only after an inquiry into what applicants are claiming, and a determination from that inquiry that applicants are

claiming a practical application of a law of nature, a natural phenomenon, or an abstract idea. That is not the case here.

Applicants' claims are directed to circuitry. Specifically, each of claims 5-13 and 26-28 define a programmable logic resource. Applicants' specification, at ¶2, defines a programmable logic resource:

A programmable logic resource is a general-purpose integrated circuit that is programmable to perform any of a wide range of logic tasks. Known examples of programmable logic resource technology include programmable logic devices (PLDs), complex programmable logic devices (CPLDs), erasable programmable logic devices (EPLDs), electrically erasable programmable logic devices (EEPLDs), and field programmable gate arrays (FPGAs).

Moreover, each of claims 5-13 and 26-28 recite that the claimed programmable logic resource comprises "at least one multiplier implemented using digital signal processing (DSP)circuitry" with the at least one multiplier comprising "multiplication circuitry," "shifting circuitry," "adder circuitry," and "zeroing circuitry." A particular advantage and utility of the claimed programmable logic resource is the more efficient use of programmable logic within the programmable logic resource by implementing saturation and rounding in the multiply-accumulate (MAC) blocks within the DSP circuitry of the programmable logic resource. This eliminates the need to implement saturation and rounding in

the programmable logic portion of the programmable logic resources.

Nothing about applicants' claims even approaches preemption of any law of nature, natural phenomenon, or abstract idea. While a user may use the claimed structure to perform particular mathematical calculations, no calculation or formula is recited in the claims, nor is any calculation or formula preempted. Accordingly, the next inquiry -- whether the claim attempts to preempt any practical application of a law of nature, natural phenomenon, or abstract idea -- does not even arise.\*

Applicants are claiming a particular circuit arrangement, and there should be no question that that circuitry is statutory subject matter. Accordingly, applicants respectfully submit that the rejection under 35 U.S.C. § 101 should be withdrawn.

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\* There was no question, for example, when the mechanical calculating machine and later the electronic calculator were invented, that they constituted statutory subject matter, even though their only purpose was to perform mathematical operations.

Conclusion

For the reasons set forth above, applicants respectfully submit that this application is in condition for allowance. Reconsideration and prompt allowance of this application are respectfully requested.

Respectfully submitted,

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